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**PATENT APPLICATION TRANSMITTAL LETTER**  
(Large Entity)

Docket No.  
END920000094US1

TO THE ASSISTANT COMMISSIONER FOR PATENTS

Transmitted herewith for filing under 35 U.S.C. 111 and 37 C.F.R. 1.53 is the patent application of:

**David J. Alcoe**

**For: COMPLIANT LAMINATE CONNECTOR**

JC945 U.S. PTO  
09/714373



Enclosed are:

- Certificate of Mailing with Express Mail Mailing Label No. **EL396832448US**
- 4 sheets of drawings.
- A certified copy of a application.
- Declaration  Signed.  Unsigned.
- Power of Attorney
- Information Disclosure Statement
- Preliminary Amendment
- Other: Assignment and Assignment Cover Sheet

**CLAIMS AS FILED**

For	#Filed	#Allowed	#Extra	Rate	Fee
<b>Total Claims</b>	41	- 20 =	21	x \$18.00	\$378.00
<b>Indep. Claims</b>	4	- 3 =	1	x \$80.00	\$80.00
<b>Multiple Dependent Claims (check if applicable)</b>					\$0.00
				<b>BASIC FEE</b>	\$710.00
				<b>TOTAL FILING FEE</b>	\$1,168.00

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Dated:

Nov. 15, 2000

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Invention: **COMPLIANT LAMINATE CONNECTOR**

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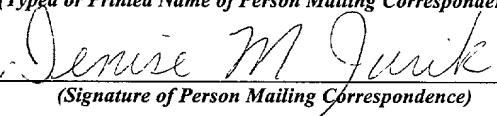
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APPLICATION  
FOR  
UNITED STATES LETTERS PATENT

APPLICANT(S) NAME: David J. Alcoe

TITLE: COMPLIANT LAMINATE CONNECTOR

DOCKET NO. END920000094US1

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## COMPLIANT LAMINATE CONNECTOR

### BACKGROUND OF THE INVENTION

#### Technical Field

The present invention relates generally to semiconductor  
5 manufacture, and more particularly, to the connection of an  
electronic device to external circuitry.

#### Related Art

As illustrated in Fig. 1, which depicts a related art module 10, a printed circuit card 12 is conventionally connected to a substrate 14, such as a chip package, using a plurality of solder ball connections 16. However, because the card 12 and the substrate 14 expand at different rates when exposed to a thermal stimulus, due to the difference in the coefficient of thermal expansion (CTE) of each, stresses are created within the solder ball connections 16 which often lead to solder ball fatigue, and subsequently result in failure of the module 10. This is particularly problematic in ceramic, glass/ceramic and aluminum/ceramic modules. Also, due to the flexibility of organic substrate modules, thermal-driven warpage may further exacerbate the problem. Accordingly, there exists a need in the industry to solve these and other problems.

## SUMMARY OF THE INVENTION

A first general aspect of the present invention provides an electronic device, comprising: a first substrate; a second substrate; and a flexible connector attached between the first and second substrates by a plurality of contacts on a first and a second surface of the connector.

A second general aspect of the present invention provides a connector system, comprising: a flexible substrate; a plurality of contacts formed on a first surface of the substrate; and a plurality of contacts formed on a second surface of the substrate, wherein select contacts on the first surface of the substrate are off-set from select contacts on the second surface of the substrate.

A third general aspect of the present invention provides a method of forming an electronic device, comprising: providing a flexible connector having a plurality of contacts on a first surface and a plurality of contacts on a second surface; and attaching the flexible connector between a first substrate and a second substrate via the contacts.

A fourth general aspect of the present invention provides a method of forming an electronic device, comprising: providing a first substrate; providing a second substrate; providing a flexible connector having a plurality of contacts on a first

surface of the connector and a plurality of contacts on a second surface of the connector, wherein select contacts on the first and second surface of the connector are off-set; and attaching the contacts on the first surface of the connector to the first substrate and the contacts on the second surface of the connector to the second substrate.

The foregoing and other features of the invention will be apparent from the following more particular description of the embodiments of the invention.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

The embodiments of this invention will be described in detail, with reference to the following figures, wherein like designations denote like elements, and wherein:

Fig. 1 depicts a cross-sectional view of a related art module;

Fig. 2 depicts a cross-sectional view of a module in accordance with the present invention;

Fig. 3A depicts the module of Fig. 2 experiencing stresses in the Z direction;

Fig. 3B depicts the flexible shear-compliant interconnection during bending;

Fig. 4 depicts an enlarged cross-sectional view of a

flexible shear-compliant interconnection in accordance with a first embodiment of the present invention;

Fig. 5 depicts an enlarged cross-sectional view of the flexible shear-compliant interconnection in accordance with a 5 second embodiment of the present invention;

Fig. 6 depicts an enlarged cross-sectional view of the flexible shear-compliant interconnection in accordance with a third embodiment of the present invention;

Fig. 7 depicts an enlarged cross-sectional view of the 10 flexible shear-compliant interconnection in accordance with a fourth embodiment of the present invention;

Fig. 8 depicts an enlarged cross-sectional view of the module in accordance with a fifth embodiment of the present 15 invention;

Fig. 9 depicts an enlarged view of a channel between the stiffener frame and the laminate in accordance with the fifth 20 embodiment of the present invention; and

Fig. 10 depicts an enlarged cross-sectional view of the module in accordance with a sixth embodiment of the present 25 invention.

#### **DESCRIPTION OF THE PREFERRED EMBODIMENTS**

Although certain embodiments of the present invention will

be shown and described in detail, it should be understood that various changes and modifications may be made without departing from the scope of the appended claims. The scope of the present invention will in no way be limited to the number of constituting components, the materials thereof, the shapes thereof, the relative arrangement thereof, etc. Although the drawings are intended to illustrate the present invention, the drawings are not necessarily drawn to scale.

Referring to the drawings, Fig. 2 shows a cross-sectional view of a module 20 in accordance with the present invention. The module 20 includes a substrate 22, such as a chip package, or other component, and a printed circuit card 24. The chip package 22 and the printed circuit card 24 are connected by a flexible shear-compliant connector or interconnection 26. The interconnection 26 includes a substrate or laminate 28 and a plurality of contacts, or in this example, ball grid array (BGA) connections 30, on the top and bottom surface of the laminate 28. The BGA connections 30 are wetted between a top bonding pad 40 of both the chip package 22 and the card 24, and a bottom bonding pad 42 of the laminate 28, using techniques known in the art. The top and bottom bonding pads 40, 42 comprise copper, or other similarly used material. The contacts 30 may alternatively comprise solder columns, etc.

The chip package 22 comprising glass/ceramic has a CTE of approximately 3 ppm/ $^{\circ}$ C, aluminum/ceramic has a CTE of approximately 5-6 ppm/ $^{\circ}$ C, a HyperBGA<sup>TM</sup> (International Business Machines Corp.) laminate has a CTE of approximately 10-12 ppm/ $^{\circ}$ C, 5 epoxy glass has a CTE of approximately 17-18 ppm/ $^{\circ}$ C, and the CTE of other packages, such as chip-scale or wafer-scale packages, can vary greatly. The card 24 has a CTE of approximately 16-22 ppm/ $^{\circ}$ C. However, due to the flexible nature of the laminate 28 of the interconnection 26, the effects of the CTE mismatch between the various kinds of chip packages 22 and the printed circuit card 24 are minimized. As a result, the occurrence of 10 solder ball fatigue is likewise minimized.

In particular, a large portion of the thermally created shear stress is spread throughout the length of the laminate 28, rather than being concentrated within the individual BGA 15 connections 30. The flexible nature of the laminate 28 is further enhanced by selectively placing critical BGA connections 20 30 in staggered or off-set positions on the top and bottom surfaces of the laminate 28. Note that not all BGA connections 30 need to be staggered to obtain an optimal solder ball fatigue life. For ceramic components, the critical BGA connections 30 are located at the far corners, or the far DNP (distance to 25 neutral point), and may be staggered at that location.

Alternatively, for organic components, the critical BGA connections 30 are located under the die region of the laminate 28, and may be staggered at that location. The BGA connections 30 are off-set by approximately the thickness of the laminate 28.

5 This provides the laminate 28 with additional flexibility in the Z direction, as illustrated in Figs. 3A and 3B. In particular, Fig. 3A shows the module 20 during bending, wherein the chip package 22 and the card 24 deform in the Z direction, thereby applying stresses to the interconnection 26, as illustrated.

10 However, due to the flexible nature of the laminate 28, the interconnection 26 can rotate, flex, or bend upwards and downwards as needed, in response to stresses in the X, Y and Z directions created by the CTE mismatch between the chip package 22 and the circuit card 24, without transmitting the stresses into the critical BGA connections 30, as further illustrated in Fig. 3B.

15 Additionally, because the laminate 28 absorbs most of the shear stresses within the module 20, the total "stand-off," or the distance between the top BGA connection 30 and the bottom BGA 20 connection 30, does not need to be as high as conventionally required to reduce the stresses and solder ball fatigue. For instance, the total stand-off may be in the range of approximately 14-60 mil. A lower stand-off produces a module 20

wherein the chip package 22 and the printed circuit card 24 are closer together, which provides improved electrical performance, lower inductance, etc.

As illustrated in Fig. 4, and in accordance with a first embodiment, the laminate 28 includes a core 31 comprising copper-invar-copper (CIC), or other similarly used material, such as copper, stainless steel, nickel, iron, molybdenum, etc. The core 31 has a thickness in the range of approximately 1-3 mil., e.g., 2 mil. The choice of core 31 material will depend upon the material within the chip package 22 being attached thereto. For a ceramic chip package 22, having a relatively low CTE, (approximately 5-6 ppm/ $^{\circ}$ C), the overall CTE of the laminate 28 may be about midway between the card 24 and the chip package 22. Therefore, in this example the overall CTE of the laminate 28 may be approximately 10-12 ppm/ $^{\circ}$ C. This provides improved distribution of stress, and therefore a reduction of stresses within the BGA connections 30 and the interconnection 26.

Accordingly, the core 31 may be a material having a low CTE, such as copper-invar-copper. If the chip package 22 has an in-plane CTE that nearly matches the card 24, then the laminate 28 may comprise a material having a similar CTE to provide additional flexibility to absorb shear and warpage stresses of either the chip package 22, the card 24, or both. In the event the card 24

has a CTE of approximately 17 ppm/ $^{\circ}$ C, the core 31 may comprise copper, having a similar CTE.

The core 31 is surrounded by a flexible dielectric layer 32.

The dielectric layer 32 is a shear compliant material which is also capable of bending or flexing in the Z direction, such as polyimide, PTFE (polytetrafluoroethylene), an epoxy dielectric material, e.g., FR4, etc. The dielectric layer 32 on each side of the core 31 has a thickness in the range of approximately 1-5 mil., e.g., 3 mil. A plated through hole (PTH) 34 is formed

through the dielectric layer 32 using conventional techniques. A solder mask 36 may then be deposited over the dielectric layer 32 using a process known in the art. The solder mask 36 has a thickness in the range of approximately 1-3 mil., e.g., 2 mil. The solder mask 36 may cover the PTH 34 to prevent solder wicking. Alternatively, the solder mask 36 may also fill the PTH 34 during deposition, which acts as a reinforcing material therein. A plurality of solder balls 38 are then wetted to the bottom bonding pad 42 on the surface of the dielectric layer 32, using a process known in the art.

Fig. 5 illustrates an alternative configuration for the interconnection 26 in accordance with a second embodiment. In particular, the BGA connections 30 are moved away from the PTH 34, which further reduces the stresses on the PTH 34, and a

connection 44 is formed over the dielectric layer 32. In this example, the connection 44 is formed between the BGA connection 30 on the top right side of the interconnection 26 and the PTH 34, and between the BGA connection 30 on the bottom left side of the interconnection 26 and the PTH 34. The connection 44 comprises a plated copper material, which has been formed and plated using a process known in the art. This provides for routing of the electrical connection from the BGA connection 30 on the top right side of the interconnection 26 to the BGA connection 30 on the bottom left side of the interconnection 26 through copper circuitry (illustrated by the cross hatching). This feature is particularly helpful when producing a "fan-out" wiring scheme, wherein the BGA connections 30 of the printed circuit card 24 have a greater pitch, or closer spacing, than the BGA connections 30 of the chip package 22. The solder mask 36 may then be formed over the top of the connection 44 as mentioned above.

Fig. 6 illustrates an alternative configuration for the interconnection 26 in accordance with a third embodiment. In particular, a ground shield 46 is formed over the top surface of each layer of solder mask 36. This provides improved impedance control for the module 26, which is particularly beneficial for use with high performance applications, such as high speed

network switches and servers.

Fig. 7 illustrates an alternative configuration for the interconnection 26 in accordance with a fourth embodiment. In particular, the interconnections 26 illustrated in Figs. 4-6 may be formed without the core 31. As shown in Fig. 7, the laminate 28 comprises a single layer of dielectric material 32, such as polyimide, or other similar material, having copper circuitry (as illustrated by the cross hatching) on either side. The circuitry is covered by the solder mask 36, which has openings for the BGA connections 30. The circuitry on one side of the laminate 28 would form a ground plane, and the other side would form a fan-out configuration. The circuitry on each side of the laminate 28 would be connected through the PTH 34.

In accordance with a fifth embodiment, Fig. 8 shows a stiffener frame 48 which surrounds the laminate 28 of the flexible shear-compliant interconnection 26. The stiffener frame 48 comprises a high temperature plastic material, having a minimal channel 52 depth (refer to Fig. 9). In other words, only a small portion of the stiffener frame 48 overlaps the flexible laminate 28 to allow for easier assembly, and subsequent removal of the frame 48 from the laminate 28 after the module 20 is assembled. The stiffener frame 48 provides for easier handling of the interconnection 26 and assists in maintaining a relatively

planar laminate 28 during manufacture.

For example, with the aid of the stiffener frame 48, the module 20 may be assembled by first placing the laminate 28 over a plurality of solder balls 38, utilizing a conventional reflow process. After the BGA connections 30 are formed on a first side of the laminate 28, the process is repeated to form the BGA connections 30 on the other side of the laminate 28 thereby forming the flexible shear-compliant interconnection 26 (as illustrated in Figs. 4-7). The interconnection 26 may then be placed on the printed circuit card 24, such that the BGA connections 30 are aligned with the top bonding pads 40 of the printed circuit card 24. The chip package 22 is then placed on top of the flexible shear-compliant interconnection 26, such that the BGA connections 30 are aligned with the top bonding pads 40 of a connecting area 23 of the chip package 22. The connecting area 23, which allows the BGA connections 30 to wet to the chip package 22, comprises copper, nickel/gold plated copper, or other similarly used materials. Thereafter, a single conventional reflow process is needed to form the interconnections 26, using a process known in the art. The stiffener frame 48 may then be removed to produce the finished module 20.

The interconnection 26 and the stiffener frame 48 allow for the preassembly of all the BGA connections 30 on the laminate 28

without having to individually place each solder ball 38 onto the chip package 22 or card 24, which would otherwise be required.

This allows, for example, for the use of a socket or land grid array for test and burn-in before assembly with BGA connections

5 30. Furthermore, the interconnection 28 and the stiffener frame 48 assist in the formation of the BGA connections 30 on the laminate 28 in a pre-aligned orientation prior to connection of the chip package 22 and/or printed circuit card 24, which reduces manufacturing time. Additionally, the interconnection 28 and the 10 stiffener frame 48 enable the formation of the module 20 with only one reflow process, rather than multiple reflow processes for each BGA connection 30, which further reduces thermally generated stresses and damage within the BGA connections 30 and the chip package 22.

15 As will be understood by those skilled in the art, the module 20 may be assembled in various other ways. For instance, the laminate 28, having BGA connections 30 attached thereto, could be attached to the chip package 22 using a high melting point solder, such as a solder material having a melting point 20 above 280°C, e.g., a conventional tin/lead solder having a low amount of tin, etc. Thereafter, the laminate 28, having BGA connections 30 attached thereto, could be attached to the printed circuit card 24 using a low melting point solder, such as a

solder material having a melting point below 250°C, e.g., a conventional tin/lead eutectic solder material, a lead free solder material, etc. Alternatively, the BGA connections 30 may be formed on the chip package 22 and the card 24, and the

5 laminate 28 may be attached therebetween, and so on.

Fig. 10 illustrates a sixth embodiment of the present invention. In particular, a stiffener 50, which assists in maintaining a planar laminate 28, may be adhesively attached to the surface of the laminate 28, using an acrylic adhesive material 49, such as Pyralux™ (DuPont), an epoxy, such as 10 Sylgard™ (Dow-Corning), a thermal adhesive, such as a silicon made by Dow-Corning, or General Electric, etc. In this manner, the module 20 will have a gradual variation of in-plane CTE from the chip package 22 to the interconnection 26 and finally to the 15 card 24. Accordingly, the potential for thermal warpage, which results from components having varied in-plane CTE values, will be reduced. The thermal conductivity of the laminate 28 combined with the stiffener 50 can provide additional heat spreading and thermal dissipation of heat from the chip package 22 to ambient air, acting as a heat sink. This is particularly useful when 20 constructing a module 20 having a fan-out wiring scheme. As illustrated, in a fan-out wiring scheme the area of the BGA connections 30 is greater on the bottom side of the flexible

shear-compliant interconnection 26 than on the top side of the interconnection 26.

The stiffener 50 comprises a material having the same or a similar CTE as that of the laminate 28, e.g., between approximately 10-20 ppm/ $^{\circ}$ C, to minimize thermally generated stresses and warpage therebetween. For instance, a stiffener 50 comprising stainless steel, (which has a CTE of approximately 10 ppm/ $^{\circ}$ C), may be used with a laminate having a CIC core 31, (which likewise has a CTE of approximately 10 ppm/ $^{\circ}$ C). Alternatively, a stiffener 50 comprising copper, (which has a CTE of approximately 17 ppm/ $^{\circ}$ C), may be used with a laminate having a copper core 31, (which likewise has a CTE of approximately 17 ppm/ $^{\circ}$ C). Using a metal stiffener 50 also provides for an enhanced thermal dissipation, acting as a heat spreading heat sink, thereby further reducing thermally generated stresses and failures within the BGA connections 30.

While this invention has been described in conjunction with the specific embodiments outlined above, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, the embodiments of the invention as set forth above are intended to be illustrative, not limiting. Various changes may be made without departing from the

spirit and scope of the invention as defined in the following claims.

## CLAIMS

I claim:

1. 1. An electronic device, comprising:
  - 2 a first substrate;
  - 3 a second substrate; and
  - 4 a flexible connector attached between the first and second
  - 5 substrates by a plurality of contacts on a first and a second
  - 6 surface of the connector.
- 1 2. The electronic device of claim 1, wherein select contacts on  
the first surface of the connector are off-set from select  
3 contacts on the second surface of the connector.
- 1 2. The electronic device of claim 1, wherein the connector  
comprises a laminate material.
- 1 2. The electronic device of claim 3, wherein the laminate  
material comprises:
  - 3 a core;
  - 4 a dielectric material surrounding the core; and
  - 5 a solder mask.

1 5. The electronic device of claim 4, wherein the laminate further  
2 includes a plated through hole.

1 6. The electronic device of claim 4, further including a  
2 connection layer between at least one contact on the first  
3 surface and at least one contact on the second surface.

1 7. The electronic device of claim 6, further including a ground  
2 shield over the connection layer.

1 8. The electronic device of claim 4, wherein the core comprises a  
2 material selected from the group consisting of: copper-invar-  
3 copper, copper, stainless steel, nickel, iron and molybdenum.

1 9. The electronic device of claim 4, wherein the dielectric  
2 material comprises polyimide.

1 10. The electronic device of claim 1, wherein the contacts  
2 comprise ball grid array connections.

1 11. The electronic device of claim 1, wherein the first substrate  
2 comprises a chip package.

1       12. The electronic device of claim 1, wherein the second  
2       substrate comprises a printed circuit board.

1       13. The electronic device of claim 1, further comprising a  
2       stiffener frame attached to the connector.

1       14. The electronic device of claim 13, wherein the stiffener  
2       frame is adhesively attached to the connector.

1       15. The electronic device of claim 13, wherein the stiffener  
2       frame surrounds a perimeter of the connector.

1       16. The electronic device of claim 13, wherein the stiffener  
2       frame is removably attached to the connector.

1       17. The electronic device of claim 13, wherein the stiffener  
2       frame is attached to a surface of the connector.

1       18. The electronic device of claim 13, wherein the stiffener  
2       frame comprises a material selected from the group consisting of:  
3       plastic, metal and ceramic.

1       19. The electronic device of claim 13, wherein the stiffener  
2       frame comprises a heat sink.

1 20. A connector system, comprising:  
2       a flexible substrate;  
3        a plurality of contacts formed on a first surface of the  
4 substrate; and  
5        a plurality of contacts formed on a second surface of the  
6 substrate, wherein select contacts on the first surface of the  
7 substrate are off-set from select contacts on the second surface  
8 of the substrate.

1       21. The connector system of claim 20, wherein the flexible  
2 substrate comprises a laminate material.

1       22. The connector system of claim 21, wherein the laminate  
2 material comprises:

3        a core;  
4        a dielectric material surrounding the core; and  
5        a solder mask.

1       23. The connector system of claim 22, wherein the laminate  
2 material further includes a plated through hole.

1       24. The connector system of claim 22, further including a  
2       connection layer between at least one contact on the first  
3       surface and at least one contact on the second surface.

1       25. The connector system of claim 22, further including a ground  
2       shield over the connection layer.

1       26. The connector system of claim 22, wherein the core comprises  
2       a material selected from the group consisting of: copper-invar-  
3       copper, copper, stainless steel, nickel, iron and molybdenum.

1       27. The connector system of claim 22, wherein the dielectric  
2       material comprises polyimide.

1       28. The connector system of claim of 20, wherein the contacts  
2       comprise ball grid array connections.

1       29. The connector system of claim 20, further including a  
2       stiffener frame.

1       30. The connector system of claim 29, wherein the stiffener frame  
2       is removably attached to the flexible substrate.

1 31. A method of forming an electronic device, comprising:  
2       providing a flexible connector having a plurality of  
3 contacts on a first surface and a plurality of contacts on a  
4 second surface; and  
5       attaching the flexible connector between a first substrate  
6 and a second substrate via the contacts.

1 32. The method of claim 31, wherein the flexible connector  
2 comprises a laminate material.

1 33. The method of claim 31, wherein the contacts comprises ball  
2 grid array connections.

1 34. The method of claim 31, wherein select contacts on the first  
2 surface of the flexible connector are off-set from select  
3 contacts on the second surface of the flexible connector.

1 35. The method of claim 31, wherein the first substrate comprises  
2 a chip package.

1 36. The method of claim 31, wherein the second substrate  
2 comprises a printed circuit board.

1       37. A method of forming an electronic device, comprising:  
2           providing a first substrate;  
3           providing a second substrate;  
4           providing a flexible connector having a plurality of  
5        contacts on a first surface of the connector and a plurality of  
6        contacts on a second surface of the connector, wherein select  
7        contacts on the first and second surface of the connector are  
8        off-set; and

9           attaching the contacts on the first surface of the connector  
10        to the first substrate and the contacts on the second surface of  
      the connector to the second substrate.

1       38. The method of claim 37, wherein the first substrate comprises  
2        a chip package.

1       39. The method of claim 37, wherein the second substrate  
2        comprises a printed circuit board.

1       40. The method of claim 37, wherein the flexible connector  
2        comprises a laminate material.

1       41. The method of claim 37, wherein the contacts comprise ball  
2        grid array connections.

## COMPLIANT LAMINATE CONNECTOR

## ABSTRACT OF THE DISCLOSURE

The present invention provides a flexible shear-compliant laminate connector having a plurality of contacts formed on a first surface and second surface of the connector, wherein select contacts on the first surface of the connector are off-set from select contacts on the second surface of the connector.

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David J. Alcole  
END9200000944US1 LRF

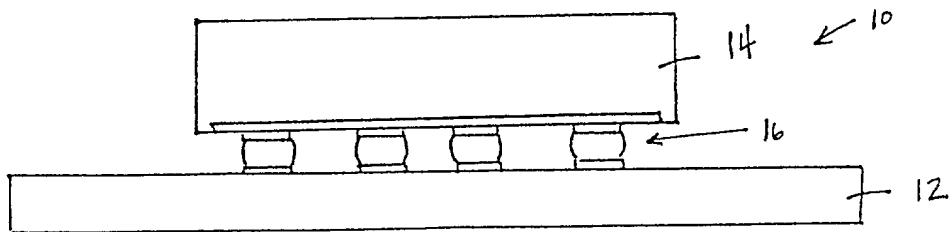


Fig. 1  
Related Art

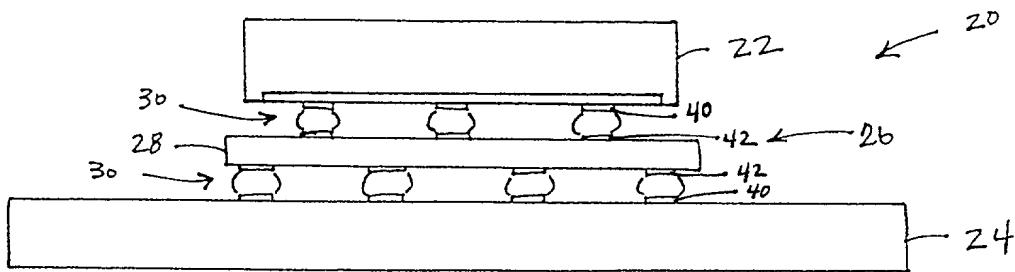


Fig. 2

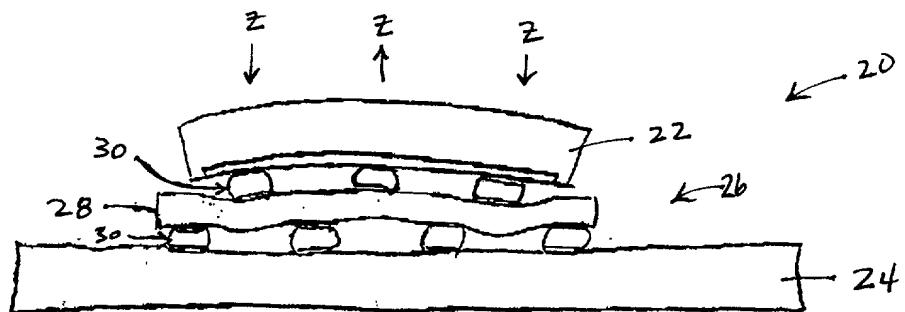


Fig. 3A

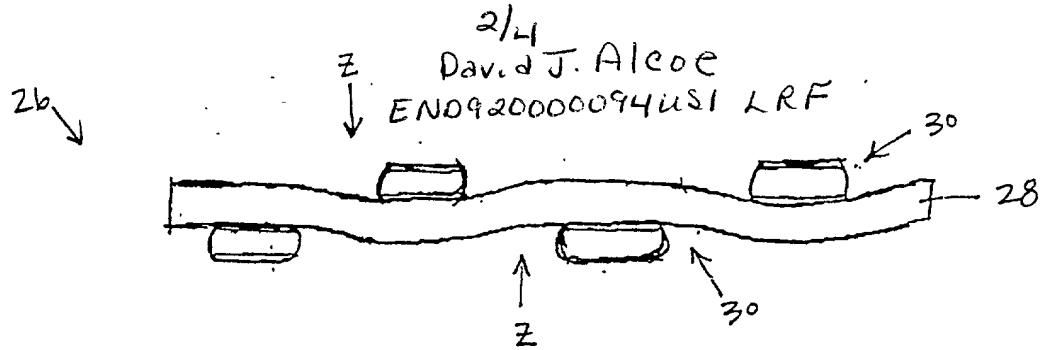


Fig. 3B

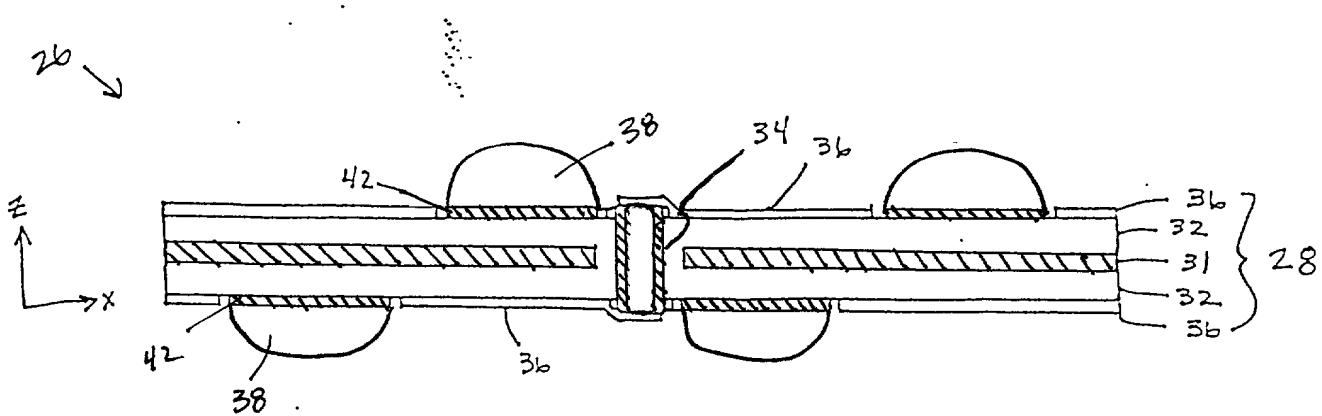


Fig. 4

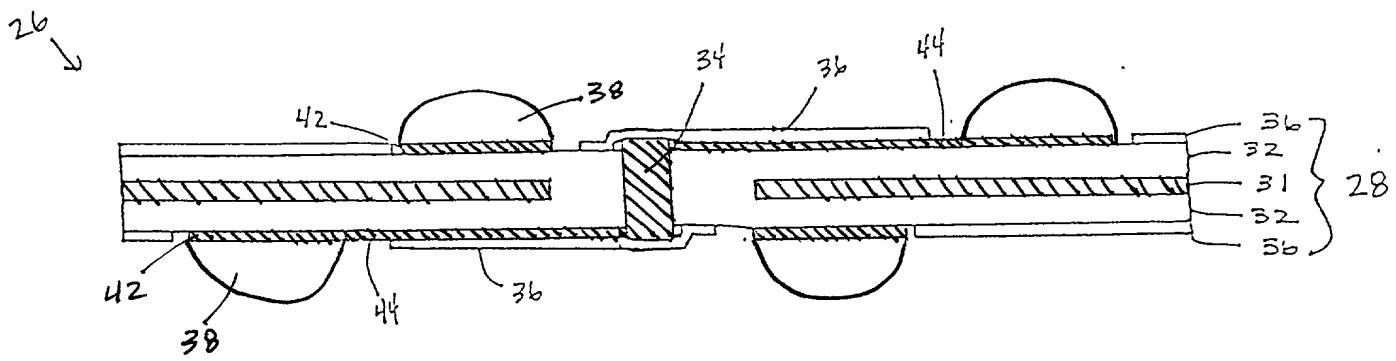


Fig. 5

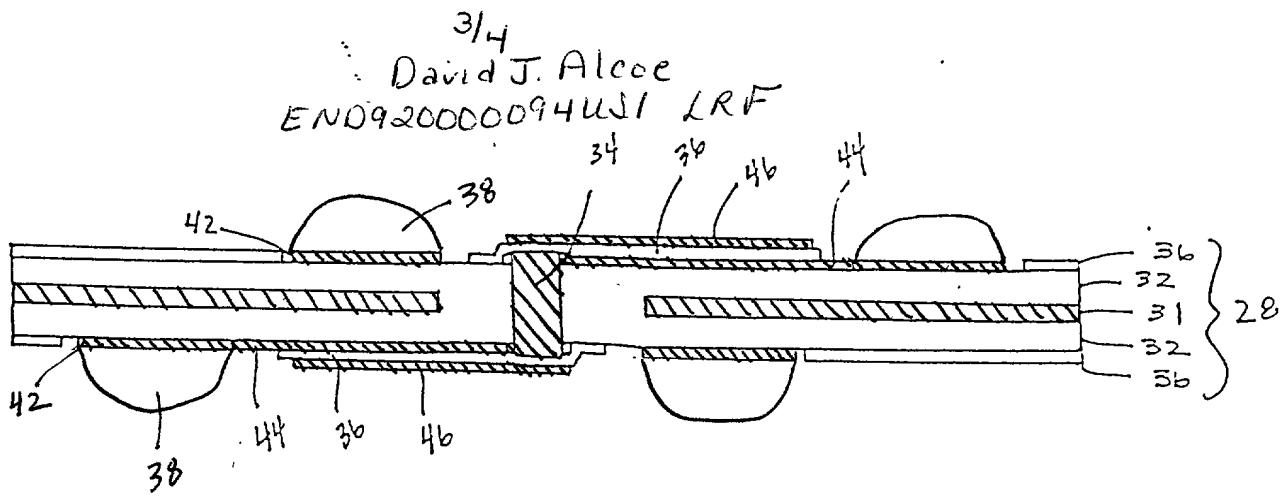


Fig. 6

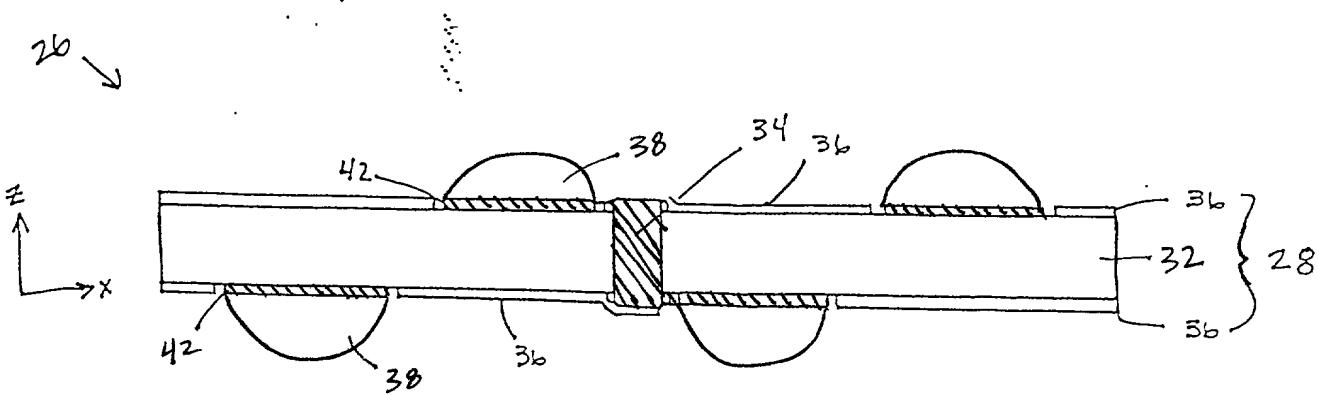


Fig. 7

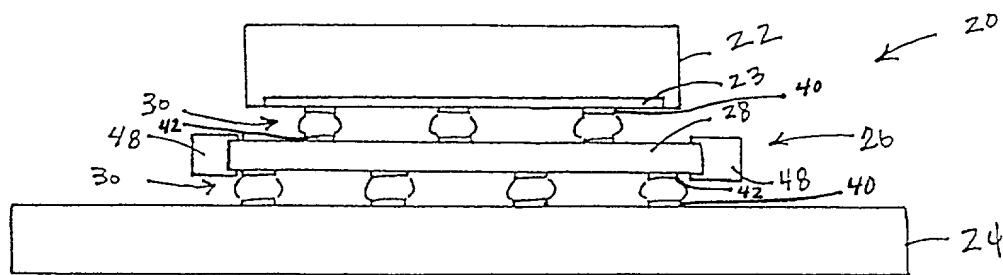


Fig. 8

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David J. Alcoe  
ENO920000094US1 LRF

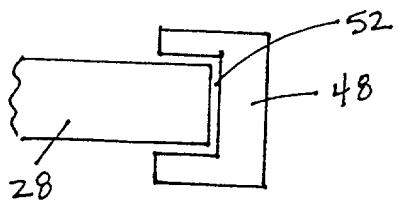


Fig. 9

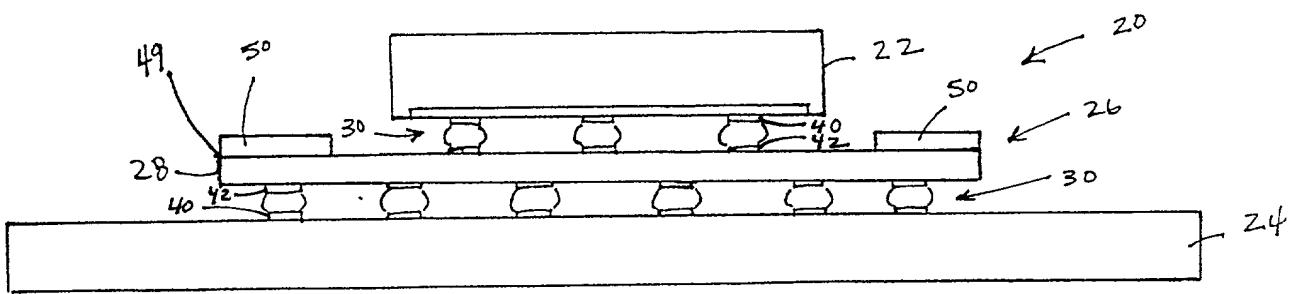


Fig. 10

Docket No.  
END920000094US1

# Declaration and Power of Attorney For Patent Application

## English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

### COMPLIANT LAMINATE CONNECTOR

the specification of which

(check one)

is attached hereto.

was filed on \_\_\_\_\_ as United States Application No. or PCT International Application Number \_\_\_\_\_  
and was amended on \_\_\_\_\_  
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

### Prior Foreign Application(s)

### Priority Not Claimed

(Number)	(Country)	(Day/Month/Year Filed)	<input type="checkbox"/>
(Number)	(Country)	(Day/Month/Year Filed)	<input type="checkbox"/>
(Number)	(Country)	(Day/Month/Year Filed)	<input type="checkbox"/>

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

---

(Application Serial No.)

---

(Filing Date)

---

(Application Serial No.)

---

(Filing Date)

---

(Application Serial No.)

---

(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

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(Application Serial No.)

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(Filing Date)

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(Status)

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(patented, pending, abandoned)

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(Application Serial No.)

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(Filing Date)

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(Status)

---

(patented, pending, abandoned)

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(Application Serial No.)

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(Filing Date)

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(Status)

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(patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

**POWER OF ATTORNEY:** As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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**Lawrence R. Fraley - 26,885**

**John R. Pivnichny - 43,001**

**Arthur J. Samodovitz - 31,297**

**William H. Steinberg - 28,540**

**Christopher A. Hughes - 26,914**

**Edward A. Pennington - 32,588**

**John E. Hoel - 26,279**

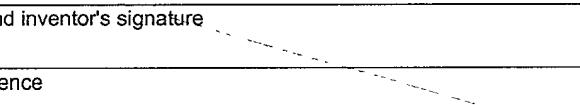
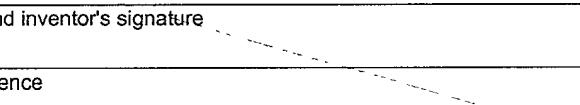
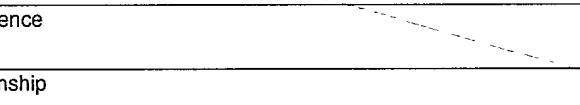
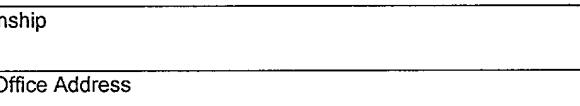
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Full name of second inventor, if any 	
Second inventor's signature 	Date
Residence 	
Citizenship 	
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